

### REMARKS

Claim 1 has been canceled and claims 2 and 13 have been amended, claims 4, 8, 9, 17 and non-elected claims 20 to 23 have previously been canceled, leaving claims 2, 3, 5 to 7 and 10 to 19 active in this application.

Claims 2 to 5, 10, 12 to 16, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Tani (U.S. 5,468,993). The rejection is respectfully traversed.

Claim 2 now includes some of the features of prior claims. More specifically, claim 2 requires the specific structure of the power distribution metallization as discussed at page 17, lines 8 to 27. This structure electrically conductive substantially coplanar, laterally disposed films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an electrically conductive seed metal layer attached to said electrically insulating overcoat and said metal-filled vias, at least one stress-absorbing film over said seed metal layer of sufficient thickness to reliably absorb mechanical, thermal and impact stresses and an outermost ~~film being~~ non-corrodible and metallurgically attachable electrically conductive layer. No such features are taught or suggested by Yamasaki et al., Tani or any proper combination of these references. Furthermore, there is clearly no teaching or suggestion in either reference to combine them in the manner suggested in the Office action even were the combination of references to teach or suggest the claimed invention, which it does not.

Claims 3 to 5, 10, 12 to 16, 18 and 19 depend from claim 2 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 2.

In addition, claim 3 further limits claim 2 by requiring that the chip be selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electrical device fabrication. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 5 further limits claim 2 by requiring that the integrated circuit comprise multi-layer metallization, at least one of the layers made of pure or alloyed copper, aluminum, nickel, or refractory metals. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 10 further limits claim 2 by requiring that leadframe segments be shaped as leads solderable to outside parts. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 12 further limits claim 2 by requiring a wire bond to the electrical conductors connecting the network lines with the second plurality of segments. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 13 further limits claim 2 by requiring that the at least one stress-absorbing metal layer selected from a group consisting of copper, nickel, aluminum, tungsten, titanium molybdenum, chromium, and alloys thereof. No such feature is taught or suggested in the

combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 14 further limits claim 2 by requiring that the outermost metal layer be selected from a group consisting of pure or alloyed gold, palladium, silver, platinum, and aluminum. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 16 further limits claim 15 by requiring that the bonding wire be selected from a group consisting of pure or alloyed gold, copper, and aluminum. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 18 further limits claim 2 by requiring that the network of lines be electrically further connected to selected segments suitable for outside electrical contact. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 19 further limits claim 2 by requiring that the network of lines, together with the metal-filled vias, provide the power distribution function between the active circuit components. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Tani further in view of Applicant's Admitted Prior Art (AAPA).

Claim 7 depends from claim 2 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 2 since (AAPA).

does not overcome the deficiencies in the other references as noted in connection with claim 2.

Claim 7 further limits claim 2 by requiring that the leadframe comprise a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, AAPA or any proper combination of these references.

Claims 6, 11 and 15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Tani in view of Wolf et al. publication. The rejection is respectfully traversed.

Claims 6, 11 and 15 depend from claim 2 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 2 since the Wolf publication fails to overcome the deficiencies in Yamasaki et al. as noted above.

Claim 6 further limits claim 2 by requiring that the overcoat comprise materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

Claim 11 further limits claim 2 by requiring solder balls attached to the electrical conductors connecting the network lines with the second plurality of segments. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

Claim 15 further limits claim 2 by requiring that the conductors be bonding wires.

No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

The propriety of the finality of the rejection is questioned since the rejection is a first rejection after filing of an RCE.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



Jay M. Cantor  
Attorney for Applicant(s)  
Reg. No. 19,906

Texas Instruments Incorporated  
P. O. Box 655474, MS 3999  
Dallas, Texas 75265  
(301) 424-0355 (Phone)  
(972) 917-5293 (Phone)  
(301) 279-0038 (Fax)